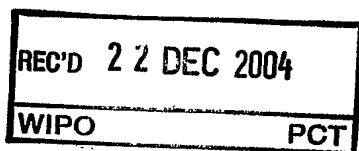




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Patentanmeldung Nr. Patent application No. Demande de brevet n°

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Anmeldung Nr:  
Application no.: 03104871.3 ✓  
Demande no:

Anmeldetag:  
Date of filing: 22.12.03 ✓  
Date de dépôt:

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A semiconductor substrate with solid phase epitaxial regrowth with reduced depth  
of doping profile and method of producing same

In Anspruch genommene Priorität(en) / Priority(ies) claimed /Priorité(s)  
revendiquée(s)  
Staat/Tag/Aktenzeichen/State/Date/File no./Pays/Date/Numéro de dépôt:

Internationale Patentklassifikation/International Patent Classification/  
Classification internationale des brevets:

H01L21/265

Am Anmeldetag benannte Vertragstaaten/Contracting states designated at date of  
filing/Etats contractants désignées lors du dépôt:

AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LU MC NL  
PT RO SE SI SK TR LI



A semiconductor substrate with solid phase epitaxial regrowth with reduced depth of doping profile and method of producing same

The present invention relates to the method of producing a semiconductor device comprising:

- a) providing a semiconductor substrate
- b) providing an insulating layer on a top surface of the semiconductor substrate
- 5 c) making an amorphous layer in a top layer of the semiconductor substrate by a suitable implant
- d) implanting a dopant into the semiconductor substrate through said insulating layer to provide the amorphous layer with a predetermined doping profile
- e) applying a solid phase epitaxial regrowth action to regrow the amorphous
- 10 layer and activate the dopant.

Such a method is known from US-A-6,063,682. According to this prior art document, heavy ions are implanted into a silicon substrate. The implanted heavy ions create  
15 an amorphous layer at the top surface of the substrate. The amorphous layer is free of channels. Then, a silicon implanting step is performed to create an excess of vacancies to interstitials within a top layer of the substrate. Since the amorphized silicon layer is free of channels, the depth of implant is mainly restricted to this amorphized silicon layer.

In the implanting step, e.g., boron (B) is used at a dose within a range of  $10^{13}$   
20 to  $10^{15} \text{ cm}^{-2}$  at an energy level of less than 15 keV. As shown in the figures of this prior art document, the boron implant has a peak value at a substantial distance from the top surface of the silicon substrate. As will be shown in detail below, this results in a poor conductivity profile at the top layer, say at a distance up to 10 nm from the top surface, within the silicon substrate.

25

It is an object of the present invention to provide a method of producing a semiconductor device as stated at the outset that results in a better conductivity profile at the top layer of the device.

To that end, the present invention provides a method as defined above wherein, in action d), the implanting is performed such that the doping profile has a peak value located within the insulating layer.

By performing this latter action, the top layer of the silicon substrate forms a  
5 junction with an improved sheet resistance and significantly reduced junction depth. A practical junction depth reduction is expected to be up to 30%.

In an embodiment, the dopant is activated to provide the amorphous layer after action e) with a conductivity profile with a peak conductivity value located substantially at the top surface.

10 The amorphous layer may be made in a Si semiconductor substrate by means of at least one of Ge, GeF<sub>2</sub>, Si, Xe or Ar atoms. If Ge atoms are used, a dose of 10<sup>15</sup> atoms/cm<sup>2</sup> and an energy of between 2 and 30 keV may be applied.

The present invention also relates to a semiconductor device made by a solid phase epitaxial regrowth technique, comprising a top layer at a surface of a semiconductor  
15 substrate with a conductivity profile with a peak conductivity value substantially at the surface.

In another embodiment the invention relates to a metal oxide semiconductor device comprising such a device.

Moreover, the invention relates to an apparatus provided with such a  
20 semiconductor device or such a metal oxide semiconductor device.

Now, the present invention will be illustrated with reference to some drawings, which are only intended to illustrate the present invention and not to limit its scope. The scope is only limited by the definition of the claims as annexed to this description, and its technical equivalents.

25

Figs. 1a-1f show different stages of producing a semiconductor device in accordance with the present invention.

Fig. 2 shows an example of a dopant concentration and a conductivity profile  
30 as a function of depth in a semiconductor substrate in accordance with a method known from the prior art.

Fig. 3 shows an Rs-sheet resistance for some p-type junctions with three different original amorphous depths within a semiconductor device, as obtained with a method known from the prior art.

Fig. 4 shows similar profiles as figure 2, however, as obtained with the method of the present invention.

5 In the description to follow, same reference numbers refer to same elements in all figures. Figures 1a-1f refer to producing a metal oxide semiconductor device in which the present invention is used. However, as will be evident to a person skilled in the art, the inventive features may be applied in the production of any other type of semiconductor device where shallow junctions are desired.

10 Figure 1a shows a semiconductor substrate 1 of a p-type. Field oxide regions 3 are provided on a top surface of the semiconductor substrate 1. At certain locations, a thin oxide layer 5 is provided by a technique known to a person skilled in the art. The thin oxide layer 5 can later be used as the gate oxide layer within the MOS device to be produced. However, the present invention is not restricted to the application of a thin oxide layer 5 to  
15 obtain the desired effect as will become clear from the description below.

The structure of figure 1a is provided with a suitable photo resist layer 30 having an opening above the thin oxide layer 5. Then, an implanting action is performed to produce an n-well 11 within the substrate 1.

20 The thin oxide layer 5 may be removed and be substituted by a new, fresh oxide layer to be later on used as the gate oxide layer in the MOS device to be produced. However, here it is assumed that the thin oxide layer 5 remains in place. As shown in figure 1c, on top of the thin oxide layer 5, a polysilicon layer 13 is provided, later to be used as the gate of the MOS device to be produced.

25 An amorphization implant 15 is performed to produce an amorphous layer in the top of the substrate 1. The depth of the implant that defines the depth of the amorphous layer is indicated with reference number 17. The implant 15 to produce this amorphous layer may be performed with Ge, GeF<sub>2</sub> or Si. However, other atoms, like xenon, argon or indium, may be applied instead. By this implant, the channels in the silicon substrate 1 are eliminated in the amorphous layer.

30 This step of producing the amorphous layer is followed by a subsequent dopant implant, e.g., with boron. Since there are no channels within the amorphous layer, the dopant implant atoms, like boron, will not penetrate substantially deeper into the silicon substrate 1 than the amorphous layer. The depth of this subsequent dopant implant is indicated with reference number 19. It is to be understood that the depth of implant 19 is only

slightly larger than the depth of the amorphous layer 17. The distances between the dashed line 17 and the top surface and the distance between the dashed line 19 and the top surface of substrate 1 are not on scale. They are only drawn to illustrate the principle of the present invention.

5 Now, reference is made to figure 2.

Figure 2 shows the top of the silicon substrate, the depth of the amorphous layer 17 and the depth of the implant of boron (as an example) 19. The boron profile corresponds to the boron profile as shown in prior art document US-A-6,063,682.

10 A next action is to apply a so called low temperature approach, i.e., a solid phase epitaxial regrowth (SPER) technique. In SPER, the silicon crystal is first pre-amorphized, then doped and finally regrown at a typical temperature between 550° C and 750° C. By this temperature action, the amorphous layer is regrown and the dopant (e.g., boron) is activated. The main advantages of SPER are limited dopant diffusion (hardly beyond the amorphous layer 17) and above solid solubility dopant activation.

15 Experiments by the present inventor have shown that for a boron profile as indicated in figure 2, after the temperature activation, a conductivity profile as indicated in figure 2 results. That is, the conductivity within a top layer that corresponds with the earlier amorphous layer 17, is rising with increasing depth from the semiconductor substrate surface to a peak value at a certain distance indicated with a dashed line 20 in figure 2. At a depth  
20 further than the dashed line 20, the conductivity falls. Behind the dash line 17, which corresponds to the earlier depth of the amorphous layer, the conductivity dramatically falls since they are hardly activated dopant atoms.

The distance between the dashed line 20 and the semiconductor substrate surface may be between 2-7 nm. Thus, the conductivity of the upper most top layer is not  
25 ideal. It is believed that this is due to poor boron activation because of a too high boron concentration in this upper most top layer of the substrate.

Figure 3 shows some results of other experiments to further illustrate the reduced conductivity in the upper most top layer of the semiconductor substrate.

30 Figure 3 shows the dependence of Rs-sheet resistance for a p-type junction with three different original amorphous depths: i.e., 9, 14 and 22 nm, respectively, versus those of a boron implant:  $5 \cdot 10^{14}$ ,  $10^{15}$ ,  $1.5 \cdot 10^{15}$ ,  $3 \cdot 10^{15}$ , and  $10^{16}$  ions/cm<sup>2</sup> of identical implant energy of 1.5 keV, respectively. The depths of 9, 14 and 22 nm, respectively, are the junction depths. As shown, a dose of  $5 \cdot 10^{14}$  ions/cm<sup>2</sup> is too low to offer a decent amount of dopants for junction activation. An increment of the dose up to  $10^{15}$  ions/cm<sup>2</sup> supplies enough dopants

for maximum junction activation. An additional increment of the dose up to  $3 \cdot 10^{15}$  ions/cm<sup>2</sup> does not substantially affect the sheet resistance value. However, further incrementing the dose up to, e.g.,  $1 \cdot 10^{16}$  ions/cm<sup>2</sup> reduces the boron activation within the junction, as can be seen by a higher sheet resistance value. Apparently, a dopant dose above a certain level  
5 reduces the performance of the junction.

To solve this problem, the present invention proposes to provide a different dopant profile as will be illustrated with reference to figure 4. On top of the semiconductor substrate there will be thin oxide layer 5 (or any other suitable insulating layer). This thin oxide layer 5 that may have a thickness of 2-4 nm, together with a suitable dose and energy  
10 of the dopant, e.g., boron, is used to produce a dopant profile such that the peak of the dopant profile is located within the oxide layer 5. Preferably, the highest value of the dopant concentration within the semiconductor device at the semiconductor device surface is selected such that the maximum obtainable conduction by these dopants is located substantially at the semiconductor substrate surface, as shown in figure 4. Then, there is no  
15 upper most top layer within the semiconductor substrate 1 with a reduced sheet resistance.

In order to obtain the dopant profile as indicated in figure 4, in an example, boron may be used with a relatively low energy, i.e. less than 5 keV, more preferably lower than 1.5 keV, at a standard dose of the order of  $10^{15}$  ions/cm<sup>2</sup>. The activation of the junction and an optional silicide formation (not explained in detail here since it is not relevant to the  
20 present invention) during the SPER process takes place with a typical temperature between 550 and 700° C during a period of typical by 1 minute. The thickness of the resulting conduction layer, i.e. between the Si surface and line 17, may be 7-12 nm.

By applying the inventive method, the junction as produced will have almost the same conductivity over its entire depth which is significantly reduced. It is expected that  
25 the junction depth may be reduced by an amount up to 30% in comparison with prior art methods.

Moreover, a junction with a box-like junction profile will result. The activation of dopants is within the original amorphous semiconductor layer and the top part of the junction will not suffer from a too high dopant concentration.

30 Moreover in some applications, the process flow may be simplified by the present method. I.e., in typical prior art processes insulating layers on top of the semiconductor substrate are removed before dopant implantation. Here, however, if such an insulating layer already exists on top of the substrate, it is intentionally used in the process.

The proposed junction formation can be used for p-type junctions, i.e., e.g. by using boron. However, the invention can equally well be applied for n-type junctions. Moreover the inventive solution can be applied for both n- and p-nodes simultaneously.

Now, with reference to figures 1d-1f, the completion of the semiconductor device to be produced will be explained.

As shown in figure 1d, after the SPER process, likely doped regions 18 result that will become source/drain extension regions of the MOS transistor on the substrate 1. The depth of this doped regions 18 will be substantially equal to the depth of the earlier amorphous layer 17.

On top of the structure, a spacer material 21 is deposited. The spacer material 21 may be silicon dioxide. However, other spacer materials may be used, as is known to a person skilled in the art.

The spacer material 21 is etched with a suitable etchant and such, that only side spacers 23 adjacent to the polysilicon layer 13 remain. See figure 1e. This is all prior art and need no further explanation here. Note that, due to the etch process, only a portion of the thin oxide layer 5 remains, i.e., the portion below the polysilicon layer 13 and the portions below the side spacers 23. The portions of the thin oxide layer 5 elsewhere are removed by the etch process.

A further ion implant action is performed as shown in figure 1f. In the embodiment shown, this is a  $p^+$  implant 29 to produce a  $p^+$  source region 27 and a  $p^+$  drain region 25. These source and drain regions 27, 25 extend deeper in the substrate 1 than the earlier doped regions 18. The side spacers 23 act as a mask to save portions of the earlier doped regions 18 from this latter  $p^+$  implant 29. Thus, extension regions 18 remain after this action.

As is known to a person skilled in the art, the manufacture of the MOS device is completed by, e.g., providing a suitable silicide process to form silicide on the drain 25, the source 27 and the polysilicon layer 13 which acts as a gate. This latter silicide process is known to a person skilled in the art and not shown in figure 1f.

## CLAIMS:

1. Method of producing a semiconductor device comprising:
  - a) providing a semiconductor substrate
  - b) providing an insulating layer on a top surface of the semiconductor substrate
  - c) making an amorphous layer in a top layer of said semiconductor substrate by a  
5 suitable implant
  - d) implanting a dopant into said semiconductor substrate through said insulating layer to provide said amorphous layer with a predetermined doping profile
  - e) applying a solid phase epitaxial regrowth action to regrow said amorphous layer and activate said dopant
- 10 wherein  
in action d), said implanting is performed such that said doping profile has a peak value located within said insulating layer.
2. Method according to claim 1, wherein said dopant is activated to provide said  
15 amorphous layer after action e) with a conductivity profile with a peak conductivity value located substantially at said top surface.
3. Method according to claim 1 or 2, wherein said semiconductor substrate is a Si substrate and action c) is performed with at least one of Ge, GeF<sub>2</sub>, Si, Xe or Ar atoms.  
20
4. Method according to claim 3, wherein said action c) is performed with Ge at a dose of 10<sup>15</sup> atoms/cm<sup>2</sup> and an energy of between 2 and 30 keV.
5. Method according to any of the preceding claims, wherein said action d) is  
25 performed with B at an energy of less than 5 keV.
6. Method according to claim 5, wherein said action d) is performed with B and a dose of 10<sup>15</sup> atoms/cm<sup>2</sup>.

7. Method according to claim 6, wherein action d) is performed at a temperature of 550-700 °C during about 1 minute.

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8. Semiconductor device made by a solid phase epitaxial regrowth technique,  
5 comprising a top layer at a surface of a semiconductor substrate with a conductivity profile with a peak conductivity value located substantially at said surface.

9. Metal oxide semiconductor device comprising a device as claimed in claim 8.

10 10. Apparatus provided with a semiconductor device as claimed in claim 8 or 9.

## ABSTRACT:

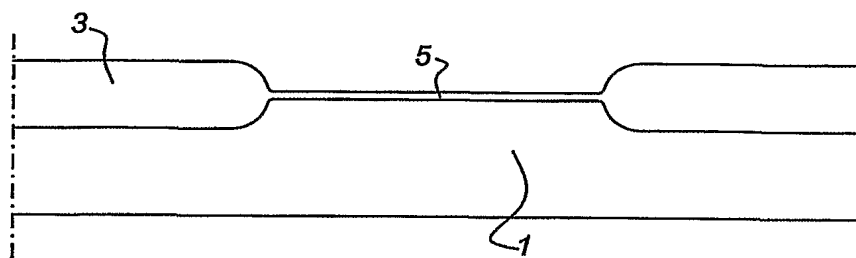
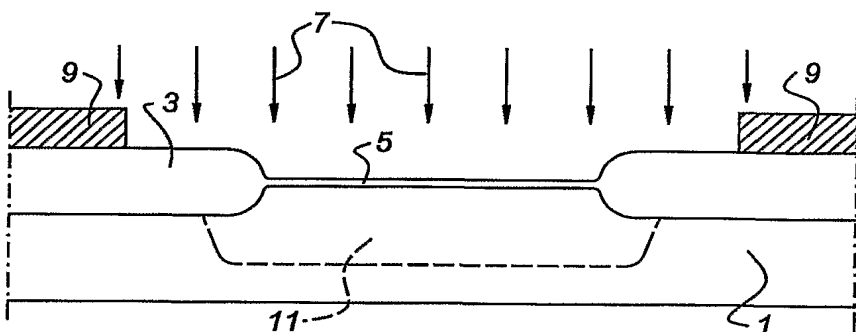
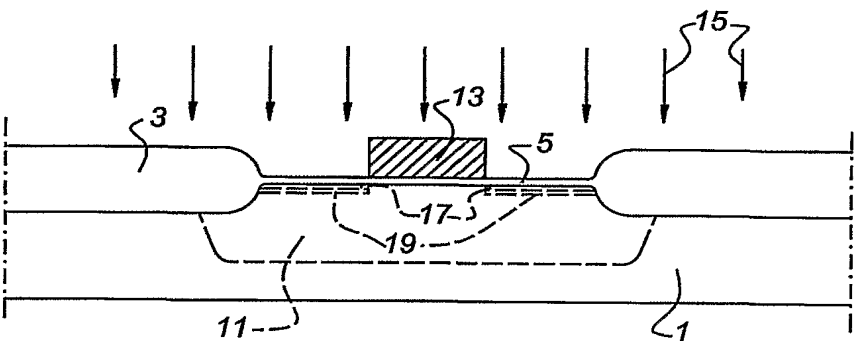
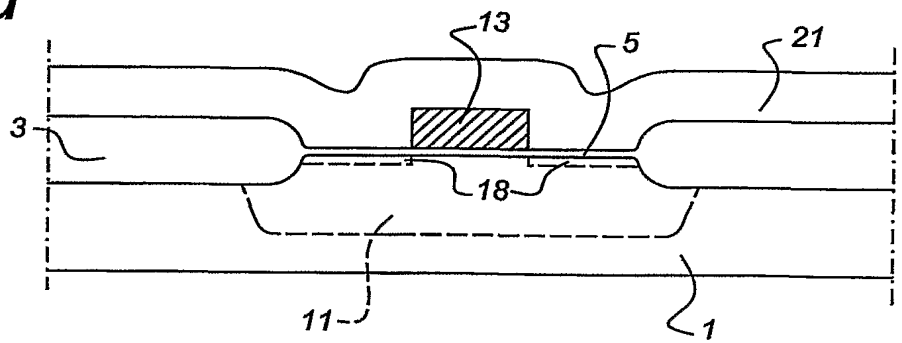
Method of producing a semiconductor device in accordance with:

- a) providing a semiconductor substrate
- b) providing an insulating layer on a top surface of the semiconductor substrate
- c) making an amorphous layer in a top layer of said semiconductor substrate by a  
5 suitable implant
- d) implanting a dopant into said semiconductor substrate through said insulating  
layer to provide said amorphous layer with a predetermined doping profile, said implanting  
being performed such that said doping profile has a peak value located within said insulating  
layer
- 10 e) applying a solid phase epitaxial regrowth action to regrow said amorphous  
layer and activate said dopant.

Fig. 4



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**Fig 1a****Fig 1b****Fig 1c****Fig 1d**

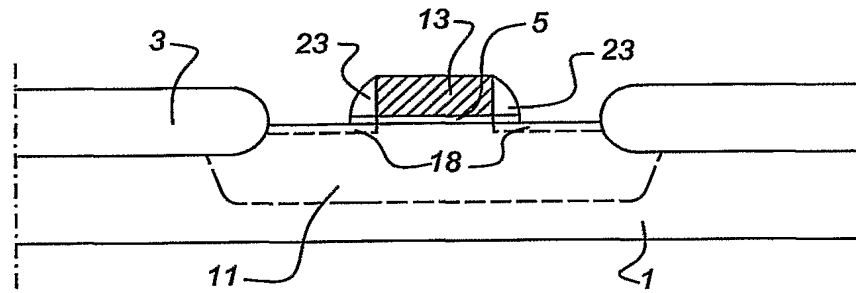
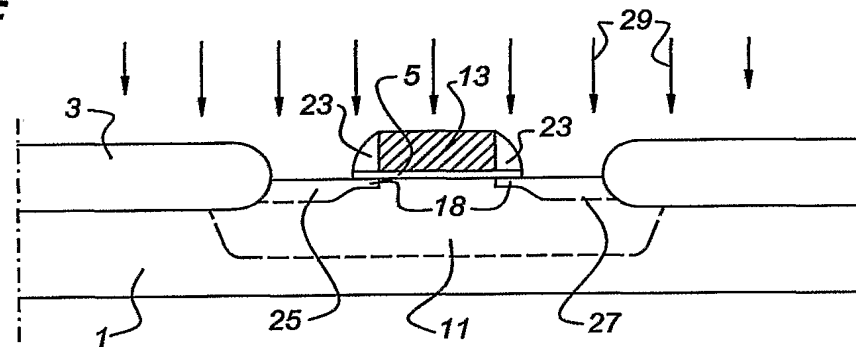
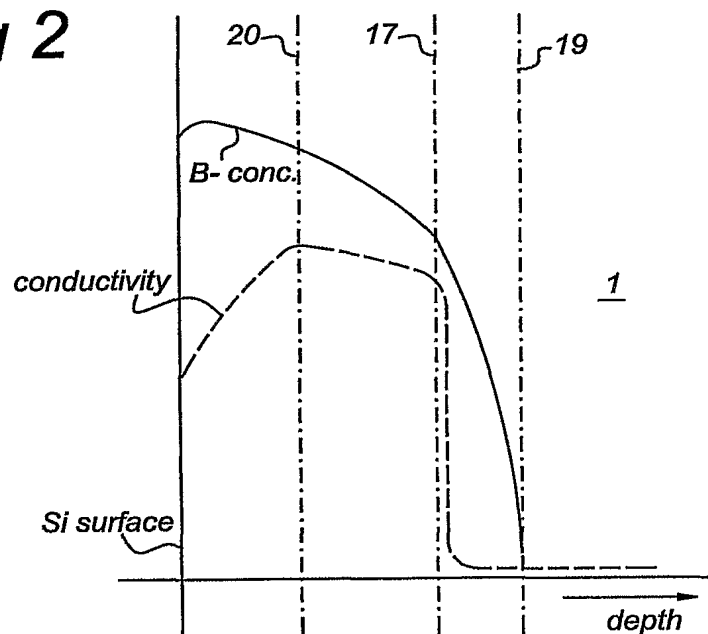
**Fig 1e****Fig 1f****Fig 2**

Fig 3

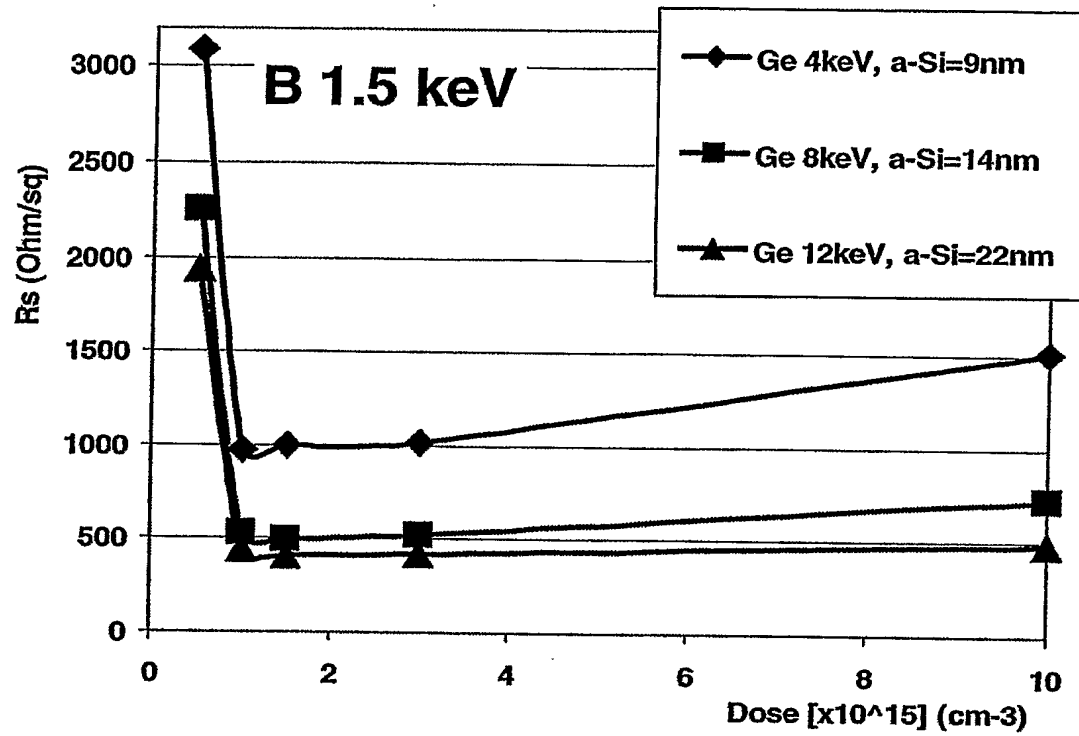
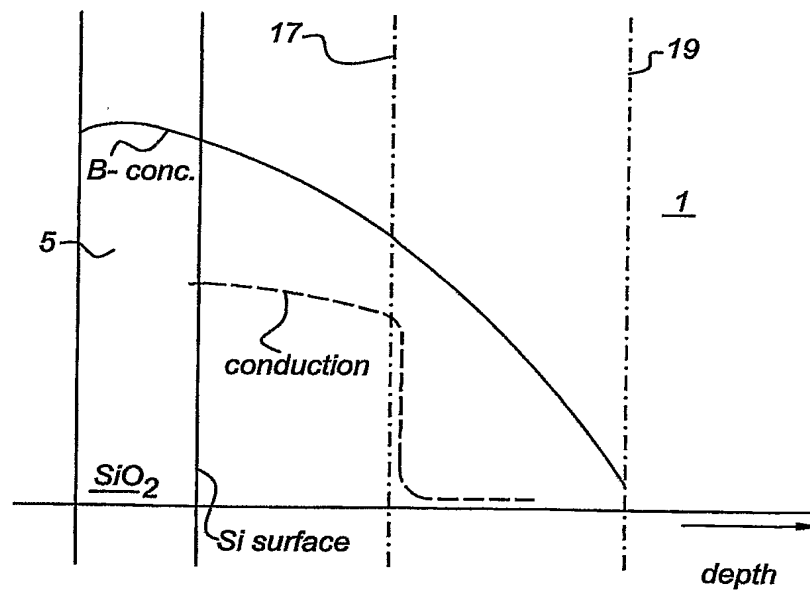


Fig 4



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